Amendments to the Claims:

This following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (original) A method of managing traffic over a network comprising:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;

performing a policing function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit;

performing a congestion control function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core;

performing a scheduling function in a third core of the digital signal processing integrated circuit, wherein the third core processes data generated by the second core; and

performing a shaping function in a fourth core of the digital signal processing integrated circuit, wherein the fourth core processes data generated by the third core.

2. (currently amended) A method of claim 1 comprising:

receiving incoming traffic from the network in [[a]] the digital signal processing integrated circuit having at least 128K bytes of on-chip memory;

performing a first traffic management function on the incoming traffic to the digital signal processing integrated circuit in [[a]] the first core of the digital signal processing integrated circuit; and

performing a second traffic management function in [[a]] the second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core.

3. (previously presented) The method of claim 2 wherein a traffic management function comprises sorting the traffic by class of service, policing traffic to not exceed boundary of a bandwidth of a channel, and scheduling traffic.

4. (original) The method of claim 3 wherein the scheduling traffic is based on priority queuing, first in first out queuing, class based queuing, round robin, waiting round robin, earlier deadline first, weighted fair queue, deficit round robin, or modified deficit round robin.

5. (original) The method of claim 2 wherein there is no direct communication path between the first core and the second core.

6. (original) The method of claim 2 wherein the data generated by the first core is passed to the second core using a mailbox.

7. (original) The method of claim 2 wherein the first core and second core are synchronized using an interrupt mechanism with a plurality of timers.

8. (original) A method of managing traffic over a network comprising:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;

performing a first portion a traffic management function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit; and

performing a second portion the traffic management function on the incoming traffic to the digital signal processing integrated circuit in a second core of the digital signal processing integrated circuit, wherein the first and second portions of the traffic management function are performed in parallel by the first and second cores of the digital signal processing integrated circuit.

9. (original) A method of managing traffic over a network comprising:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;

performing a first traffic management function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit;

performing a first portion of a second traffic management function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core; and

performing a second portion of the second traffic management function in a third core of the digital signal processing integrated circuit, wherein the first and second portions of the second traffic management function are performed in parallel by the second and third cores of the digital signal processing integrated circuit.

10–44. (canceled)

45. (previously presented) The method of claim 1 wherein the digital signal processing integrated circuit comprises an analog-to-digital converter.

46. (previously presented) The method of claim 8 wherein the digital signal processing integrated circuit comprises an analog input.

47. (previously presented) The method of claim 9 wherein the digital signal processing integrated circuit comprises a digital-to-analog converter.

48. (previously presented) The method of claim 5 wherein the data generated by the first core is passed to the second core using a mailbox.

49. (previously presented) The method of claim 5 wherein the first core and second core are synchronized using an interrupt mechanism with a plurality of timers.

50. (previously presented) The method of claim 1 wherein the digital signal processing integrated circuit performs a method comprising:

from the incoming traffic, receiving a first entry to be stored in a memory location of the at least 128K bytes of on-chip memory, wherein the first entry has a time stamp value, represented in a floating point format, and a data value;

dividing the time stamp value of the first entry into two or more portions, a first time stamp portion and a second time stamp portion;

providing a first pointer memory structure, referred to by a first pointer address, having a head and a body, wherein the head comprises a bit map field and a pointer-to-body field;

providing a second pointer memory structure having a head and a body, wherein the head comprises a bit map field and a pointer-to-body field;

storing a second pointer address in the body of the first pointer memory structure based on the first time stamp portion; and

indicating the position in the head of the first pointer, wherein the second pointer address points to the second pointer memory structure.

51. (previously presented) The method of claim 8 wherein the digital signal processing integrated circuit performs a method comprising:

from the incoming traffic, receiving a first entry to be stored in a memory location of the at least 128K bytes of on-chip memory, wherein the first entry has a time stamp value, represented in a floating point format, and a data value;

dividing the time stamp value of the first entry into two or more portions, a first time stamp portion and a second time stamp portion;

providing a first pointer memory structure, referred to by a first pointer address, having a head and a body, wherein the head comprises a bit map field and a pointer-to-body field;

providing a second pointer memory structure having a head and a body, wherein the head comprises a bit map field and a pointer-to-body field;

storing a second pointer address in the body of the first pointer memory structure based on the first time stamp portion; and

indicating the position in the head of the first pointer, wherein the second pointer address points to the second pointer memory structure.

52. (previously presented) The method of claim 9 wherein the digital signal processing integrated circuit performs a method comprising:

from the incoming traffic, receiving a first entry to be stored in a memory location of the at least 128K bytes of on-chip memory, wherein the first entry has a time stamp value, represented in a floating point format, and a data value;

dividing the time stamp value of the first entry into two or more portions, a first time stamp portion and a second time stamp portion;

providing a first pointer memory structure, referred to by a first pointer address, having a head and a body, wherein the head comprises a bit map field and a pointer-to-body field;

providing a second pointer memory structure having a head and a body, wherein the head comprises a bit map field and a pointer-to-body field;

storing a second pointer address in the body of the first pointer memory structure based on the first time stamp portion; and

indicating the position in the head of the first pointer, wherein the second pointer address points to the second pointer memory structure.

53. (previously presented) The method of claim 1 wherein the digital signal processing integrated circuit performs a method comprising:

from the incoming traffic, receiving an entry comprising a binary time stamp;

converting the binary time stamp into a time stamp, represented by a mantissa and an exponent, having a first time stamp portion and a second time stamp portion;

providing a first pointer memory structure stored in the at least 128K bytes of on-chip memory, referenced using a first pointer address and having a head and a body, wherein the head comprises a bit map field comprising two or more bits and the body comprises two or more memory positions, each bit in the bit map field representing one of the two or more memory positions;

initializing the two or more bits of the head of the first pointer memory structure to a first state;

when storing a second pointer address in a first memory position of the two or more memory positions, changing a first bit of the two or more bits of the head of the first pointer memory structure to a second state; and

when storing the second pointer address in a second memory position of the two or more memory positions, changing a second bit of the two or more bits of the head of the first pointer memory structure to the second state.

54. (previously presented) The method of claim 8 wherein the digital signal processing integrated circuit performs a method comprising:

from the incoming traffic, receiving an entry comprising a binary time stamp;

converting the binary time stamp into a time stamp, represented by a mantissa and an exponent, having a first time stamp portion and a second time stamp portion;

providing a first pointer memory structure stored in the at least 128K bytes of on-chip memory, referenced using a first pointer address and having a head and a body, wherein the head comprises a bit map field comprising two or more bits and the body comprises two or more memory positions, each bit in the bit map field representing one of the two or more memory positions;

initializing the two or more bits of the head of the first pointer memory structure to a first state;

when storing a second pointer address in a first memory position of the two or more memory positions, changing a first bit of the two or more bits of the head of the first pointer memory structure to a second state; and

when storing the second pointer address in a second memory position of the two or more memory positions, changing a second bit of the two or more bits of the head of the first pointer memory structure to the second state.

55. (previously presented) The method of claim 9 wherein the digital signal processing integrated circuit performs a method comprising:

from the incoming traffic, receiving an entry comprising a binary time stamp;

converting the binary time stamp into a time stamp, represented by a mantissa and an exponent, having a first time stamp portion and a second time stamp portion;

providing a first pointer memory structure stored in the at least 128K bytes of on-chip memory, referenced using a first pointer address and having a head and a body, wherein the head comprises a bit map field comprising two or more bits and the body comprises two or more

memory positions, each bit in the bit map field representing one of the two or more memory positions;

initializing the two or more bits of the head of the first pointer memory structure to a first state;

when storing a second pointer address in a first memory position of the two or more memory positions, changing a first bit of the two or more bits of the head of the first pointer memory structure to a second state; and

when storing the second pointer address in a second memory position of the two or more memory positions, changing a second bit of the two or more bits of the head of the first pointer memory structure to the second state.

56–58. (canceled)

59. (previously presented) The method of claim 8 wherein there is no direct communication path between the first core and the second core, the data generated by the first core is passed to the second core using a mailbox, and the data generated by the first core is passed to the second core using a mailbox.

60. (previously presented) The method of claim 9 wherein there is no direct communication path between the first core and the second core, the data generated by the first core is passed to the second core using a mailbox, and the data generated by the first core is passed to the second core using a mailbox.

61. (previously presented) The method of claim 1 wherein the digital signal processing integrated circuit comprises a phase-locked loop circuit.

62. (previously presented) The method of claim 8 wherein the digital signal processing integrated circuit comprises a phase-locked loop circuit.

63. (previously presented) The method of claim 9 wherein the digital signal processing integrated circuit comprises a phase-locked loop circuit.

64. (previously presented) The method of claim 1 comprising:
using the first core to configure a first timer circuit;
enabling a second timer and third timer using the first timer;
using the second timer to trigger a first interrupt for the first core; and
using the second time to trigger the first interrupt for the second core.

65. (previously presented) The method of claim 64 comprising:
using the first core to configure a fourth timer circuit;
enabling a fifth timer and sixth timer using the fourth timer;
using the fifth timer to trigger the first interrupt for the third core; and
using the sixth timer to trigger the first interrupt for the fourth core.

66. (previously presented) The method of claim 8 comprising:
using the first core to configure a first timer circuit;
enabling a second timer and third timer using the first timer;
using the second timer to trigger a first interrupt for the first core; and
using the third timer to trigger the first interrupt for the second core.

67. (previously presented) The method of claim 9 comprising:
using the first core to configure a first timer circuit;
enabling a second timer and third timer using the first timer;
using the second timer to trigger a first interrupt for the first core; and
using the third timer to trigger the first interrupt for the second core.